Abstract

Providing shared memory data transfer apparatus which enables data transfers between a plurality of bus masters and a shared memory by using a simple, small-scale control circuit

In order to solve the problem, the shared memory data transfer apparatus includes a plurality of master I/Fs respectively connected to the masters, write data buffers connected to the master I/Fs for retaining data written from the masters to the shared memory, read data buffers connected the master interfaces for retaining data read from the shared memory to the masters, a command FIFO provided between the master interfaces and the shared memory for storing commands from the masters directed to the shared memory in a first-in, first-out fashion, and a shared memory I/F for controlling data transfers from the write buffers to the shared memory or data transfers from the shared memory to the read buffers in accordance with commands fetched from the command FIFO.